Question Bank(Microcontroller (BELE0-F99)

1. The special function registers are maintained in the next 128 locations after the general-purpose data storage and stack.

A.True
B.False

Answer: A

2. Which data memory control and handle the operation of several peripherals by assigning them in the category of special function registers?

a. Internal on-chip RAM
b. External off-chip RAM
c. Both a & b
d. None of the above

ANSWER: (a) Internal on-chip RAM

3. Why is the speed accessibility of external data memory slower than internal on-chip RAM?

a. Due to multiplexing of lower order byte of address-data bus
b. Due to multiplexing of higher order byte of address-data bus
c. Due to demultiplexing of lower order byte of address-data bus
d. Due to demultiplexing of higher order byte of address-data bus

ANSWER: (a) Due to multiplexing of lower order byte of address-data bus

4. Which operations are performed by the bit manipulating instructions of boolean processor?

a. Complement bit
b. Set bit
c. Clear bit
d. All of the above

ANSWER: (d) All of the above

5. Which control signal/s is/are generated by timing and control unit of 8051 microcontroller in order to access the off-chip devices apart from the internal timings?

a. ALE
b. PSEN

c. RD & WR
d. All of the above

ANSWER: (d) All of the above

6. Which register usually store the output generated by ALU in several arithmetic and logical operations?

a. Accumulator
b. Special Function Register
c. Timer Register
d. Stack Pointer

ANSWER: (a) Accumulator

7) Which condition approve to prefer the EPROM/ROM versions for mass production in order to prevent the external memory connections?

a. size of code < size of on-chip program memory
b. size of code > size of on-chip program memory
c. size of code = size of on-chip program memory
d. None of the above

ANSWER: (a) size of code < size of on-chip program memory

8) Which among the below mentioned devices of MCS-51 family does not possess two 16 - bit timers/counters?

a. 8031
b. 8052
c. 8751
d. All of the above

ANSWER: (b) 8052

9) Which characteristic/s of accumulator is /are of greater significance in terms of its functionality?

a. Ability to store one of the operands before the execution of an instruction
b. Ability to store the result after the execution of an instruction
c. Both a & b
d. None of the above

ANSWER: (c) Both a & b

10) Which general purpose register holds eight bit divisor and store the remainder especially after the execution of division operation?

a. A-Register
b. B-Register
c. Registers R0 through R7
d. All of the above

ANSWER: (b) B-Register

11) How many registers can be utilized to write the programs by an effective selection of register bank in program status word (PSW)?

a. 8
b. 16
c. 32
d. 64

ANSWER: (c) 32

12) Which operations are performed by stack pointer during its incremental phase?

a. Push
b. Pop
c. Return
d. All of the above

ANSWER: (a) Push

13) Which is the only register without internal on-chip RAM address in MCS-51?

a. Stack Pointer
b. Program Counter
c. Data Pointer
d. Timer Register

ANSWER: (b) Program Counter

14) What kind of instructions usually affect the program counter?

a. Call & Jump
b. Call & Return
c. Push & Pop
d. Return & Jump

ANSWER: (a) Call & Jump

15) What is the default value of stack once after the system undergoes the reset condition?

a. 07H
b. 08H
c. 09H
d. 00H

ANSWER:(a) 07H

16) Which bit/s play/s a significant role in the selection of a bank register of Program Status Word (PSW)?

a. RS1
b. RS0
c. Both a & b
d. None of the above

ANSWER: (c) Both a & b

17) Which flags represent the least significant bit (LSB) and most significant bit (MSB) of Program Status Word (PSW) respectively?

a. Parity Flag & Carry Flag
b. Parity Flag & Auxiliary Carry Flag
c. Carry Flag & Overflow Flag
d. Carry Flag & Auxiliary Carry Flag

ANSWER: (a) Parity Flag & Carry Flag

18) Which register bank is supposed to get selected if the values of register bank select bits RS1 & Rs0 are detected to be '1' & '0' respectively?

a. Bank 0
b. Bank 1
c. Bank 2
d. Bank 3

ANSWER: (c) Bank 2

19) It is possible to set the auxiliary carry flag while performing addition or subtraction operations only when the carry exceeds _____

a. 1st bit
b. 2nd bit
c. 3rd bit
d. 4th bit

ANSWER: (c) 3rd bit

20) Which locations of 128 bytes on-chip additional RAM are generally reserved for special functions?

a. 80H to 0FFH
b. 70H to 0FFH
c. 90H to 0FFH
d. 60H to 0FFH

ANSWER: (a) 80H to 0FFH

21) Which commands are used for addressing the off-chip data and associated codes respectively by data pointer?

a. MOVX & MOVC
b. MOVY & MOVB
c. MOVZ & MOVA
d. MOVC & MOVY

ANSWER: (a) MOVX & MOVC

22) Which instruction find its utility in loading the data pointer with 16 bits immediate data?

a. MOV
b. INC
c. DEC
d. ADDC

ANSWER: (a) MOV

23) What is the maximum capability of addressing the off-chip data memory & off-chip program memory in a data pointer?

a. 8K
b. 16K
c. 32K
d. 64K

ANSWER: (d) 64K

24) Which among the below stated registers does not belong to the category of special function registers?

a. TCON & TMOD
b. TH0 & TL0
c. P0 & P1
d. SP & PC

ANSWER: (d) SP & PC

25) Which timer is attributed to the register pair of RCAP2H & RCAP2L for capture mode operation?

a. Timer 0
b. Timer 1
c. Timer 2
d. Timer 3

ANSWER:(c) Timer 2

26) Which registers are supposed to get copied into RCAP2H & RCAP2L respectively due to the transition at 8052 T2EX pin in the capture mode operation?

a. TH0 & TH1
b. TH1 & TH1
c. TH2 & TH2
d. All of the above

ANSWER: (c) TH2 & TH2

27) Which mode of timer 2 allow to hold the reload values with an assistance of RCAP2H & RCAP2L register pair?

a. 8 bit auto-reload mode
b. 16 bit auto reload mode
c. 8 bit capture mode
d. 16 bit capture mode

ANSWER: (b) 16 bit auto reload mode

28) Where should the pin 19 (XTAL1), acting as an input of inverting amplifier as well as part of an oscillator circuit, be connected under the application of external clock?

a. to XTAL2
b. to Vcc
c. to GND
d. to ALE

ANSWER: (c) to GND

29) Which port does not represent quasi-bidirectional nature of I/O ports in accordance to the pin configuration of 8051 microcontroller?

a. Port 0 (Pins 32-39)
b. Port 1 (Pins 1-8)
c. Port 2 (Pins 21-28)
d. Port 3 (Pins 10-17)

ANSWER: (a) Port 0 (Pins 32-39)

30) What is the required baud rate for an efficient operation of serial port devices in 8051 microcontroller?

a. 1200
b. 2400
c. 4800
d. 9600

ANSWER: (d) 9600

31) Which among the below mentioned functions does not belong to the category of alternate functions usually performed by Port 3 (Pins 10-17)?

a. External Interrupts
b. Internal Interrupts
c. Serial Ports
d. Read / Write Control signals

ANSWER: (b) Internal Interrupts

32) What is the constant activation rate of ALE that is optimized periodically in terms of an oscillator frequency?

a. 1 / 8
b. 1 / 6
c. 1 / 4
d. 1 / 2

ANSWER:(b) 1 / 6

33) Which output control signal is activated after every six oscillator periods while fetching the external program memory and almost remains high during internal program execution?

a. ALE
b. PSEN

c. EA
d. All of the above

ANSWER: (b) PSEN

34) Which memory allow the execution of instructions till the address limit of 0FFFH especially when the External Access (EA) pin is held high?

a. Internal Program Memory
b. External Program Memory
c. Both a & b
d. None of the above

ANSWER: (a) Internal Program Memory

35) Which value of disc capacitors is preferred or recommended especially when the quartz crystal is connected externally in an oscillator circuit of 8051?

a. 10 pF
b. 20 pF
c. 30 pF
d. 40 pF

ANSWER: (c) 30 pF

36) Why are the resonators not preferred for an oscillator circuit of 8051?

a. Because they do not avail for 12 MHz higher order frequencies
b. Because they are unstable as compared to quartz crystals
c. Because cost reduction due to its utility is almost negligible in comparison to total cost of microcontroller board
d. All of the above

ANSWER: (d) All of the above

37) Which version of MCS-51 requires the necessary connection of external clock source to XTAL2 in addition to the XTAL1 connectivity to ground level?

a. HMOS
b. CHMOS
c. CMOS
d. All of the abov

ANSWER: (a) HMOS

38) Which signal from CPU has an ability to respond the clocking value of D- flipflop (bit latch) from the internal bus?

a. Write-to-Read Signal
b. Write-to-Latch Signal
c. Read-to-Write Signal
d. Read-to-Latch Signal

ANSWER: (b) Write-to-Latch Signal

39) Which among the below mentioned statements are precisely related to quasi-bidirectional port?

a. Fixed high pull-up resistors are internally connected
b. Configuration in the form of input pulls the port at higher position whereas they get pulled lower when configured as a source current
c. It is possible to drive the pin as output at any duration when FET gets turned OFF for an input function
d. Upper pull-up FET is always OFF with the provision of 'open-drain' output pin for normal operation of port

a. A, B, C, D
b. A, B & C
c. A & B
d. C & D

ANSWER: (b) A, B & C

40) What happens when the pins of port 0 & port 2 are switched to internal ADDR and ADDR / DATA bus respectively while accessing an external memory?

a. Ports cannot be used as general-purpose Inputs/Outputs
b. Ports start sinking more current than sourcing
c. Ports cannot be further used as high impedance input
d. All of the above

ANSWER: (a) Ports cannot be used as general-purpose Inputs/Outputs

41) The upper 128 bytes of an internal data memory from 80H through FFH usually represent _____.

a. general-purpose registers
b. special function registers
c. stack pointers
d. program counters

ANSWER: (b) special function registers

42) What is the bit addressing range of addressable individual bits over the on-chip RAM?

a. 00H to FFH
b. 01H to 7FH
c. 00H to 7FH
d. 80H to FFH

ANSWER: (c) 00H to 7FH

43) What is the divisional range of program memory for internal and external memory portions respectively when enable access pin is held high (unity)?

a. 0000H – 0FFFH & 1000H – FFFFH
b. 0000H – 1000H & 0FFFH – FFFFH
c. 0001H – 0FFFH & 01FFH – FFFFH
d. None of the above

ANSWER: (a) 0000H – 0FFFH & 1000H – FFFFH

44) Consider the following statements. Which of them is/are correct in case of program execution related to program memory?

a. External Program memory execution takes place from 1000H through 0FFFFH only when the status of EA pin is high (1)
b. External Program memory execution takes place from 0000H through 0FFFH only when the status of EA pin is low (0)
c. Internal Program execution occurs from 0000H through 0FFFH only when the status of EA pin is held low (0)
d. Internal program memory execution occurs from 0000H through 0FFFH only when EA pin is held high (1)

a. A & C
b. B & D
c. A & B
d. Only A

ANSWER: (b) B & D

45) How does the processor respond to an occurrence of the interrupt?

a. By Interrupt Service Subroutine
b. By Interrupt Status Subroutine

c. By Interrupt Structure Subroutine
d. By Interrupt System Subroutine

ANSWER: (a) By Interrupt Service Subroutine

46) Which address/location in the program memory is supposed to get occupied when CPU jump and execute instantaneously during the occurrence of an interrupt?

a. Scalar
b. Vector
c. Register
d. All of the above

ANSWER: (b) Vector

47) Which location specify the storage/loading of vector address during the interrupt generation?

a. Stack Pointer
b. Program Counter
c. Data Pointer
d. All of the above

ANSWER: (b) Program Counter

48) Match the following :

a. ISS ——————————— 1. Monitors the status of interrupt pin
b. IER ——————————— 2. Allows the termination of ISS
c. RETI ——————————— 3. MCS-51 Interrupts Initialization
d. INTO ——————————— 4. Occurrence of high to low transition level

a. A-1, B-2, C-3, D-4
b. A-3, B-2, C-4, D-1
c. A-1, B-3, C-2, D-4
d. A-4, B-3, C-2, D-1

ANSWER:(c) A-1, B-3, C-2, D-4

49) What kind of triggering configuration of external interrupt intimate the signal to stay low until the generation of subsequent interrupt?

a. Edge-Triggering
b. Level Triggering
c. Both a & b
d. None of the above

ANSWER: (b) Level Triggering

50) Which among the below mentioned reasons is/are responsible for the generation of Serial Port Interrupt?

a. Overflow of timer/counter 1
b. High to low transition on pin INT1
c. High to low transition on pin INT0
d. Setting of either TI or RI flag

a. A & B
b. Only B
c. C & D
d. Only D

ANSWER: (d) Only D

51) What is the counting rate of a machine cycle in correlation to the oscillator frequency for timers?

a. 1 / 10
b. 1 / 12
c. 1 / 15
d. 1 / 20

ANSWER: (b) 1 / 12

52) Which special function register play a vital role in the timer/counter mode selection process by allocating the bits in it?

a. TMOD
b. TCON
c. SCON
d. PCON

ANSWER:(a) TMOD

53) How many machine cycle/s is/are executed by the counters in 8051 in order to detect '1' to '0' transition at the external pin?

a. One
b. Two
c. Four
d. Eight

ANSWER: (b) Two

54) Which bit must be set in TCON register in order to start the 'Timer 0' while operating in 'Mode 0'?

a. TR0
b. TF0
c. IT0
d. IE0

ANSWER: (a) TR0

55. Which among the following control/s the timer1 especially when it is configured as a timer in mode'0′, where gate and TR1 bits are attributed to be '1" in TMOD register?

a. TR1
b. External input at (INT1)
c. TF1
d. All of the above

ANSWER: (b) External input at (INT1)

56) Which timer mode exhibit the necessity to generate the interrupt by setting EA bit in IE enhancing the program counter to jump to another vector location?

a. Mode 0
b. Mode 1
c. Mode 2
d. Mode 3

ANSWER: (b) Mode 1

57. Which among the below mentioned program segments represent the correct code?

a. MOV SP, # 54 H
MOV TCON ,# 0010 0000 C
SETC ET1
SETC TR0
SJMP $
b. MOV SP, # 54H
MOV TMOD ,# 0010 0000 C
SETC ET0
SETC TR0
SJMP $
c. MOV SP, # 54 H
MOV TMOD ,# 0010 0000 C
SETC ET1
SETC TR1

SETC EA
SJMP $
d. MOV SP, # 54 H
MOV TMOD ,# 0010 0000 C
SETC ET0
SETC TR1
SETC EA
SJMP $

ANSWER: (c)

MOV SP, # 54 H
MOV TMOD ,# 0010 0000 C
SETC ET1
SETC TR1
SETC EA
SJMP $

58) What is the maximum delay generated by the 12 MHz clock frequency in accordance to an auto-reload mode (Mode 2) operation of the timer?

a. 125 μs
b. 250 μs
c. 256 μs
d. 1200 μs

ANSWER: (c) 256 μs

59) Which among the below mentioned sequence of program instructions represent the correct chronological order for the generation of 2kHz square wave frequency?

1. MOV TMOD, 0000 0010 B

2. MOV TL0, # 06H

3. MOV TH0, # 06H

4. SETB TR0

5. CPL p1.0

6. ORG 0000H

a. 6, 5, 2, 4, 1, 3
b. 6, 1, 3, 2, 4, 5

c. 6, 5, 4, 3, 2, 1
d. 6, 2, 4, 5, 1, 3

ANSWER: (b) 6, 1, 3, 2, 4, 5

60) Why is it not necessary to specify the baud rate to be equal to the number of bits per second?

a. Because each bit is preceded by a start bit & followed by one stop bit
b. Because each byte is preceded by a start byte & followed by one stop byte
c. Because each byte is preceded by a start bit & followed by one stop bit
d. Because each bit is preceded by a start byte &followed by one stop byte

ANSWER: (c) Because each byte is preceded by a start bit & followed by one stop bit

61. Why is CHMOS technology preferred over HMOS technology for designing the devices of MCS-51 family?

a. Due to higher noise immunity
b. Due to lower power consumption
c. Due to higher speed
d. All of the above

ANSWER: (d) All of the above

62. MOV A, @ R1 will:
A.copy R1 to the accumulator
B.copy the accumulator to R1
C.copy the contents of memory whose address is in R1 to the accumulator
D.copy the accumulator to the contents of memory whose address is in R1

Answer: Option C